Notice of Allowability	Application No.	Applicant(s)	
	10/751,170	DHANOA, KULWINDER	
	Examiner	Art Unit	
	Paul W. Schlie	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *arguments filed 7/17/06 and examiner initiated interview/resulting amendments of 8/17/06*.

2. ☒ The allowed claim(s) is/are *1-17 and 20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with C. Bart Sullivan on 8/17/06, whereby:

Claims 1, 5-6, 10-11 and 20 are further amended; and

Claims 18-19 are canceled.

3. The application has been amended as follows:

Claim 1. (currently amended) A memory controller, comprising:

at least one bus interface, each bus interface being for connection to at least one respective devices for receiving memory access requests;

a memory interface, for connection to a memory device; and

control logic, for placing received memory access requests into a queue of memory access requests, wherein, when a queued memory access request is a read access request which requires multiple bursts of data to be read from the memory device, the control logic calculates the number of required data bursts and a starting address for each burst, and places the respective memory access requests into the queue of memory access requests such that back-to-back SDRAM read bursts can be subsequently performed, ~~wherein the control logic determines whether the read access request is for data that can be delivered in a single burst of data, or for data that requires multiple bursts of data~~, wherein the memory access requests that require multiple bursts are queued together so read latency is incurred only once.

Claim 2. (original) A memory controller as claimed in claim 1, wherein, when a memory access request is a read access request which requires multiple bursts of data to be read from the memory device, the calculated starting address for a first of said required data bursts comprises a row address and a column address, and the calculated starting address for a second and any subsequent required data bursts comprises a column address but no row address.

Claim 3. (original) A memory controller as claimed in claim 2, wherein the calculated starting address for the first of said required data bursts further comprises a chip select indication.

Claim 4. (original) A memory controller as claimed in claim 1, comprising a plurality of bus interfaces, wherein memory access requests received from different bus interfaces may be placed into the queue of memory access requests with different priorities.

Claim 5. (currently amended) A memory controller as claimed in claim 1, comprising a plurality of bus interfaces, wherein memory access requests received from different bus interfaces may be placed into the queue of memory access requests with priorities determined in such a way as to ~~maximise~~ maximize efficient usage of a memory bus connected to the memory interface.

Claim 6. (currently amended) In a memory controller, comprising at least one bus interface, each bus interface being for connection to at east one respective devices for receiving memory access requests; and a memory interface, for connection to a memory device; the method comprising:

~~determining from a memory access request if the memory access request requires a single burst of data, or multiple bursts of data to be read from the memory device;~~

when a queued memory access request is a read access request which requires multiple bursts of data to be read from the memory device, calculating the number of required data bursts and a starting address for each burst, and

placing the respective memory access requests into a queue of memory access requests such that back-to-back SDRAM read bursts can be subsequently performed, wherein the memory access requests are queued together so read latency is incurred only once.

Claim 7. (original) A method as claimed in claim 6, comprising, when a memory access request is a read access request which requires multiple bursts of data to be read from the memory device, calculating said starting address for a first of said required data bursts comprising a row address and a column address, and calculating said starting address for a second and any subsequent required data bursts comprising a column address but no row address.

Claim 8. (original) A method as claimed in claim 7, comprising calculating said starting address for the first of said required data bursts comprising a chip select indication.

Claim 9. (original) A method as claimed in claim 6, in a memory controller comprising a plurality of bus interfaces, comprising placing memory access requests received from different bus interfaces into the queue of memory access requests with different priorities.

Claim 10. (currently amended) A method as claimed in claim 6, in a memory controller comprising a plurality of bus interfaces, comprising placing memory access requests received from different bus interfaces into the queue of memory access requests with priorities determined in such a way as to ~~maximise~~ maximize efficient usage of a memory bus connected to the memory interface.

Claim 11. (currently amended) A memory controller, comprising:

at least one first bus interface, for connection to a master device for receiving queued memory access requests and for transmitting data to the master device;

a second bus interface, for connection to a memory device, such that data can be retrieved from the memory device in data bursts;

control logic, for receiving memory access requests from the first bus interface, and for calculating a required number of data bursts needed to deal with each received memory access request; and

a queue store, for storing addresses ~~data~~ relating to each of the calculated ~~required~~ number of data bursts subsequently performed,

wherein the control logic stores data in the queue store, relating to each of the required number of data bursts, ~~and for determining if the memory access requests require a single data burst or multiple data bursts~~ wherein memory access requests that require multiple bursts are queued together so read latency is incurred only once.

Claim 12. (original) A memory controller as claimed in claim 11, wherein the control logic stores data in the queue store, relating to each of the required number of data bursts, such that the data bursts corresponding to a received memory access request can be retrieved without incurring a separate read latency for each data burst.

Claim 13. (original) A memory controller as claimed in claim 11, wherein the control logic stores data in the queue store, indicating that the required number of data bursts correspond to a single received memory access request.

Claim 14. (previously presented) A memory controller as claimed in claim 11, wherein the control logic prioritizes the memory access requests based on bus interface type, or single burst, or multiple burst.

Claim 15. (previously presented) A memory controller as claimed in claim 11, wherein the control logic determines from the memory access requests a burst length or a burst type.

Claim 16. (previously presented) A memory controller as claimed in claim 1, wherein the multiple bursts of data are provided within one successive clock cycle.

Claim 17. (previously presented) A memory controller as claimed in claim 1, wherein control logic determines if the read access requires a incrementing burst type of wrapping burst type.

Claim 18.-19. (canceled)

Claim 20. (currently amended) A method as claimed in claim 6, <u>further comprising</u> ~~wherein determining comprises~~ determining the burst length or the burst type <u>of the memory access requests</u>.

Conclusion

1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PIERRE BATAILLE
PRIMARY EXAMINER
8\25\06